ABSTRACT OF THE DISCLOSURE

A technique to track flag transitions to ensure proper timing of data transfers to and from DRAM devices. In one scheme, a queue is employed to track occurrences of read/write commands, chip select signal and flag transitions to generate a trigger signal to effect the data transfer. In another scheme, read/write command indications are replaced by a rank select signal to enable this data trigger scheme to work even in heavily loaded configurations where there is more timing skew.